We claim:

1. A memory array, comprising:

at least a first column of memory cells and a second column of memory cells, wherein the memory cells of the first column and the second column have a common logic and are associated with at least a first memory port and a second memory port;

first column bitlines in communication with the memory cells of the first column, the first column bitlines including bitlines in communication with the first memory port and the second memory port, wherein the bitlines associated with the first memory port include a bitline exchange associated with a first selected row of memory cells and the bitlines associated with the second memory port include a bitline exchange associated with a second selected row of memory cells, wherein the first selected row and the second selected row are different; and

second column bitlines in communication with the memory cells of the second column, the second column bitlines including bitlines in communication with the first memory port and the second memory port, wherein the bitlines associated with the first memory port include a bitline exchange associated with the first selected row of memory cells and the bitlines associated with the second memory port include a bitline exchange associated with the second selected row of memory cells.

2. The memory array of claim 1, further comprising a conductor situated between the first column of memory cells and the second column of memory cells and configured to be charged to a predetermined voltage.

3. The memory array of claim 1, wherein the conductor is configured to supply electrical power to the memory cells of at least one of the first column and the second column of memory cells.

4. The memory array of claim 1, wherein the memory cells of the first column and the second column have a common design.

5. The memory array of claim 1, wherein the memory cells are associated with a third memory port, and bitlines associated with the third memory port include bitline exchanges at one of the first selected row or the second selected row.

6. A memory, comprising:

an array of multi-port memory cells, the array associated with a plurality of columns of memory cells;

a plurality of bitlines in communication with the columns of memory cells, wherein the plurality of bitlines for each column of memory cells includes bitlines associated with the memory ports of the multi-port memory cells, wherein the bitlines associated with at least a first memory port include a bitline exchange associated with a first selected row of memory cells and the bitlines associated with at least a second memory port include a bitline exchange associated with a second selected row of memory cells, wherein the first selected row and the second selected row are different.

7. The memory of claim 6, further comprising a set of intercolumn conductors configured to be charged to at least one fixed voltage.

8. The memory of claim 7, wherein the set of intercolumn conductors includes conductors associated with a first voltage and a second voltage.

9. The memory of claim 7, wherein the bitlines and bitline exchanges associated with a selected memory port are defined in two conductor layers.

10. The memory of claim 6, wherein each of the columns of memory cells is of a common design.

11. The memory of claim 6, wherein each of the memory cells is of a common design.

12. A memory driver for communicating with memory cells in a column of memory cells, comprising:

a multiplexer having a control input and configured to communicate a logical value or a complement of the logical value to or from a selected memory cell in the column of memory cells; and

a controller configured to direct the multiplexer to select the logical value or the complement of the logical value based on a row address of the selected memory cell.

13. The memory driver of claim 12, wherein the controller is configured to provide a control signal to the control input of the multiplexer based on an exclusive OR function of two or more bits of the row address.

14. The memory driver of claim 13, wherein the controller includes an XOR gate.

15. The memory driver of claim 12, where the controller is configured to select the logical value of the complement of the logical value based on a number of bitline exchanges associated with the selected memory cell.

16. A method of designing a multi-port memory array, comprising:

defining a column of memory cells having bitlines associated with each of the memory ports;

associating bitline exchanges with the bitlines of at least two memory ports, wherein the bitline exchanges for the at least two memory ports are associated with different rows; and

arranging plurality of the columns of memory cells to form an array of memory cells, thereby forming a multi-port memory array.

17. A computer readable medium comprising computer executable instructions for performing the method of claim 16.

18. The method of claim 16, further comprising defining the bitlines and bitline exchanges in two conductor layers.

19. A method of reducing electrical interference in a multi-port memory, comprising:

interchanging complementary bitlines associated with a first memory port at least a first row in substantially all columns of the memory; and

interchanging complementary bitlines associated with a second memory port at at least a second row in substantially all columns of the memory, wherein the second row is different than the first row.

20. The method of claim 19, wherein the complementary bitlines associated with the first memory port are interchanged at a first set of rows and the complementary bitlines associated with the second memory port are interchanged at a

second set of rows, wherein the first set of rows and the second set of rows are different.

21. The method of claim 20, wherein the first set of rows includes even-numbered rows and the second set of rows includes odd-numbered rows.